REMARKS

Claims 1-40 stand rejected on prior art grounds and upon informalities. Applicants respectfully traverse these rejections based on the following discussion. Claims 4 and 12 are cancelled herein because the previously claimed feature is currently amended into each of the independent claims. Claim 23 is also cancelled herein. Claims 41 and 42 are newly added. Therefore, claims 1-3, 5-11 and 13-42 are all the claims presently pending in the application.

References have been made in previous amendments and Office Actions to various paragraphs of the specification of the present invention. It should be noted that the paragraph numbering on the patent application document filed by the Applicants on December 17, 2001 differs when compared to the corresponding published patent application (U.S. Patent Application Pub. 2005/0114944). For example, paragraph [0015] of the patent application as filed was apparently re-labeled as paragraph [0017] by the U.S. Patent and Trademark Office when the application was published. As mentioned on page 20 of the August 15, 2006 Amendment, reference by the Applicants to paragraph [0017] was specifically to paragraph [0017] of the published document. For consistency, all references made by the Applicants to the specification and paragraphs therein will be to the published patent document.

I. The 35 U.S.C. §112, First Paragraph, Rejection

A. Second bounded range. Claims 1-40 stand rejected under 35 U.S.C. §112, first paragraph, because "The "second bounded range" identifying the variation between multiple design is critical or essential to the practice of the invention, but in the claims(s) is not enabled in the disclosure." Specifically, the Office Action indicates that the independent claims "disclose

second bounded range representing the performance parameter variations between multiple designs. The figure 1 & 2 and accompanying disclosure do not teach how the second bounded range would be bounded between multiple designs. Further there is no disclosure of multiple design of a transistor, a resistor or a capacitor thereby identifying various models." The Applicants respectfully disagree.

As amended, each of the independent claims 1, 9, 14, 19, 24, 36 and 40 comprise the following features (or features similar thereto): (1) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range," (2) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point," (3) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit," and (4) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

Support of each these features is found throughout the specification of the present invention. Summary paragraph [0007] of the published patent application provides that the invention relates to modeling a device that has a performance parameter with bounded ranges: (1) a first bounded range has performance parameter variations within a single manufacturing process; and (2) a second bounded range has performance parameter variations due to different device designs.

This is explained in greater detailed in paragraphs [0020]-[0030] of the published patent application and Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] further explains that variations in a design of a device (that achieve the same performance point may results in different model curves (see curves 20-22 of Figure 2 representing multiple different designs for the same device). That is, curves 20-22 were based on the same target model. Thus, as explained in paragraph [0028] the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., it includes the second bounded range as claimed). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on processes windows (i.e., first bounded ranges, designated by dashed lines in Figure 2) around each of the design curves 20-22.

Specifically, as illustrated in Figures 2 and 3 and explained in paragraphs [0029]-[0030], the final target performance parameter range 30 includes all point between curves 20 and 22 (i.e., includes a second bounded range). It is further expanded to include all points between the upper edge of 27 of the processing window (i.e., the first bounded range) that is located around the most linear curve 22 and the lower edge 25 of the processing window (i.e., another first bounded range) that is located around the least linear curve 20 of the second bounded range). Thus, the final target performance parameter range also includes multiple first bounded ranges. Consequently, the Applicants submit that the bounded ranges that are included in the target

performance parameter range are enabled by the disclosure and the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. Capacitor or Resistor. Claims 1-40 further stand rejected under 35 U.S.C. §112, first paragraph, because "[t]he "capacitor" or "resistor" models amended in the claim do not have disclosed support for performance parameter like the transistor model". The Applicants respectfully disagree.

First, it should be noted that the independent claims are amended herein to refer to a device that comprises "an integrated circuit component" rather that "a device that is one of a transistor, a capacitor and a resistor". Paragraph [0017] of published patent application states the following:

> [0017] In the description to follow, reference will be made to "devices" and "products". In the preferred embodiment, "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. However, it is to be understood that the invention is also applicable to any component of any product, where the performance attributes of that component help determine the functionality of the integrated product. Examples include chemical components and subcomponents of a drug, or the insole of a shoe, or the foam insulation of a hot tub. In each example, the former is the "device" and the latter is the "product".

Thus, the disclosure is not limited the exemplary devices of a transistor, a capacitor or a resistor, but rather refers to any integrated circuit component (passive or active) or any other component of a product for that matter Thus, the independent claims are expanded to reflect the broad nature of the disclosure.

Second, the Office Action indicated that only a transistor model is enabled because a performance parameter is critical or necessary to the invention, but the disclosure only discusses exemplary performance parameters for a transistor. The Applicants respectfully disagree. As discussed above and clearly set out in paragraph [0017] of the published patent application, the device referred to in the claimed invention is an integrated circuit component (i.e., a transistor, capacitor, resistor or the like) having a performance parameter. For illustration purpose, the invention was described in terms of a transistor and an exemplary performance parameters for a transistor were discussed (e.g., voltage switchpoint (see paragraph [0018]), voltage output at a specific current (see paragraph [0024]).

Contrary to the Examiners assertion, it is not the performance parameter itself that is critical or essential to the practice of the invention, but rather that the device, whatever it may be (e.g., a transistor of an IC, resistor of an IC, insole of a shoe, foam of hot tub, etc.), has a performance parameter that is a design point. For example, in addition to mentioning the voltage switchpoint as an exemplary parameter for a transistor of an IC, paragraph [0018] of the published application also provided exemplary performance parameters for other product components (e.g., rigidity of an insole for a shoe, coefficient of thermal expansion of foam for a hot tub, etc.). Those skilled in the art would clearly recognize that other different performance parameter may be used as the design point for a transistor when implementing the claimed invention Similarly, those skilled in the art would clearly recognize that various different performance parameter may be used as the

design point for other integrated circuit components when implementing the claimed invention.

Consequently, the Applicants submit that the integrated circuit components and their various performance parameters are enabled by the disclosure and the Examiner is respectfully requested to reconsider and withdraw this rejection.

C. Computer model. Claims 1-40 further stand rejected under 35 U.S.C. §112, first paragraph, because generation of a computer model using performance parameters is not enable by the disclosure. The Applicants respectfully disagree for the same reasons as set out above in response to the enable rejection based on the second bounded range and on the capacitor/resistor.

Consequently, the Applicants submit that the computer model is enabled by the disclosure and the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. The 35 U.S.C. §112, Second Paragraph, Rejection

Claims 1-40 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These rejections are traversed as explained below.

As amended, each of the independent claims 1, 9, 14, 19, 24, 36 and 40 comprise the following features (or features similar thereto): (1) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range," (2) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point," (3) "wherein each of

said multiple different designs is directed to a variation of a single design for said integrated circuit," and (4) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

Thus, the metes and bounds of the target performance parameter range is provided as are the metes and bounds of the bounded ranges that are included in the target performance parameter range. Additionally, the amended claims clarify that the target model is created using a target performance parameter range and that this target performance parameter range includes the bounded ranges. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

Claims 14 and 24 were further rejected because, according to the Office Action, it appears from the claim language "a product having a device" that the product has only one device, such that the product and the device are equivalent for all intensive purposes. The Applicants respectfully disagree but have amended the claims to refer to "a product comprising a device". In view of the fact that it is generally understood that the use of the term "comprising" is not limiting, that the product is clearly referred to in the claims as having features not shared with the device and that the specification clearly defines the product as different from the device, the Examiner is respectfully requested to reconsider and withdraw this rejection.

Claim 14 was further rejected under 35 U.S.C. §112, second paragraph, due to a lack of antecedent basis. The Applicants respectfully disagree. Specifically, the rejection indicated "developing device goals for said device, wherein said device goals are based on [missing antecedent basis] product goal". Claim 14 does not include a limitation of developing or

providing product goals, so the limitation of "said device goals based on product goals" does not present an antecedent basis issue. In view of the foregoing the Examiner is respectfully requested to withdraw this rejection.

Claims 23 and 36 were also rejected under 35 U.S.C. §112, second paragraph. Claim 23 is cancelled herein and claim 36 is amended herein in order to overcome the rejection. In view of the foregoing the Examiner is respectfully requested to withdraw the rejection to claim 36.

III. The Prior Art Rejections

Claims 1-27 and 30-40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, et al. (U.S. Patent No. 6,269,277) hereinafter referred to as Hershenson, in view of Krivokapic, et al. (U.S. Patent No. 5,966,527), hereinafter referred to as Krivokapic, in further view of Applicant own Admission, hereinafter referred to as AAPA. Claims 28-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, in view of Krivokapic, in further view of AAPA, and in further view of Peng, et al. (U.S. Patent No. 6,028,994), hereinafter referred to as Peng. Applicants respectfully traverse these rejections based on the following discussion.

A. Independent claims 1, 9, 14, 19, 24, 36, and 40

Regarding independent claims 1, 9, 14, 19, 24, 36, 40 and 42, the Applicants submit that the cited prior art references do not teach or disclose the following claimed features: (1) "a target performance parameter range for said performance attribute"; (2) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; (3) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding

one of multiple model curves for different designs of said device that achieve a same performance point"; (4) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit"; and (5) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

Hershenson provides a system for providing automated synthesis of a globally optimal designs for a given circuit topology library, directly from user defined specifications. Specifically, referring to col. 5, line 35-col. 6, line 25, Hershenson provides that when a new semiconductor manufacturing process is initiated on the CAD system, models for the transistors (i.e., a single component of an IC) are generated. The CAD system may include posynomial models of different levels and complexity that can be selected as needed based on the design requirements. The CAD system also includes a library of circuit topologies. Topologies are generally understood to be configurations (i.e., a relative arrangements of components, parts or elements (see Merriam-Webster Online Dictionary copyright © 2005 by Merriam-Webster, Incorporated). The library is divided into groups based on multi-component device type (e.g., op-amps, amplifiers for automatic gain control, limiters, oscillators, etc.). Thus, it is understood that the library includes, for each multi-component device, one or more different topologies or different relative arrangements of the individual components (e.g., transistors) within the devices.

After a transistor model is selected, a user selects a circuit topology or group of circuit topologies for the device from the library and then selects performance specifications for the desired device (i.e., for the desired op-amp, oscillator, etc.). More specifically, for a given

multi-component device (e.g., an op-amp) the user determines the design parameters and performance specifications (see col. 10, line 35-col. 11, line 30). Each performance specification is defined in posynomial form for use in a geometric program. The system then generates a geometric program for the defined performance specification of the multi-component device, and based on a user-selected optimization mode, reformulates the geometric program as convex optimizations problems (see col. 7, lines 60-67). The program solves the geometric program for the a globally optimal design of the integrated circuit topology for the user-defined defined specifications.

Krivokapic discloses a method for simulating the behavior of a mass-produced device. Specifically, Krivokapic recognizes that a designer must consider numerous transistor attributes in predicting semiconductor behavior and that a designer often must balance conflicting attributes to achieve a desired behavior (e.g. drain-to-source current vs. drain-to source voltage curves (I/V curve)). Various prior art device simulators model designed transistor behavior. However, prior art modeling do not accurately reflect mass-produced semiconductor device and do not use semiconductor manufacturing process simulations to generate distributions of manufactured semiconductor devices (see col. 3, line 66- col. 4, line 3). Thus, Krivokapic discloses an improved method for modeling designed transistor behavior in which I/V curves are obtained and used to show how choice of semiconductor device attributes, such as channel length, effect the guard band or manufacturability of such devices (see col. 4, lines 26-34). Specifically, referring to Figure 5 and the related text, performance values are obtained from devices with different attributes (step 500). A device simulator is calibrated based on the performance values (step 501). A process simulator is calibrated based on the performance

values and the measured attributes of the devices (step 502). The process simulator is run (step 503). Then, the results of the process simulator are input into the device simulator to obtain I/V curves (step 504) and to determine the statistical worst-case I/V curves (step 505) by averaging the drain-to-source current values associated with drain to source voltage values. Parameters for device simulators are then extracted from the statistical worst-case I/V curves (step 506). The device simulator will output worst-case I/V curves in response to input parameters obtained from the statistical worst-case I/V curves (step 507) and finally, the worst case I/V curves can be compared to an ideal curve to obtain manufacturing guard bands (step 508).

Contrarily, as discussed in detail above, the claimed invention is concerned with creating a computer model using a target device model, where the target device model is created using a target performance parameter range as opposed to a single target performance point for a given performance attribute . This target range is constrained by two variables (manufacturing process and device design).

More particularly, in Hershenson, a user defines the performance specifications for a multi-component device (i.e., a circuit, such as an op-amp) and the system generates optimizes uses a CAD library to generate a globally optimal design solution for achieving the defined performance specifications (see col. 5, line 35-col. 6, line 25). Nowhere in Hershenson does it disclose a target performance parameter range. Krivokapic discloses that the results of a process simulator are input into the device simulator to obtain I/V curves (step 504) and to determine the statistical worst-case I/V curves (step 505) *by averaging* the drain-to-source current values associated with drain to source voltage values. Worst-case IV curves are just that – the worst case—and, thus, would be used to bound the range for target performance. Krivokapic does

refer to an ideal I/V curve to which the worst case I/V curves are compared to identify manufacturing guard bands. However, nowhere in Krivokapic is a target performance parameter range disclosed.

Furthermore, since neither Krivokapic, nor Hershenson teach a target performance parameter range, they necessarily also do not teach the limiting features of the target performance parameter range as claimed. That is, neither Krivokapic, nor Hershenson teach the limiting feature that the target parameter range includes multiple first bounded ranges each comprising range of performance parameter variations due to manufacturing process variations and each based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point. Nor do they teach or suggest that the target performance parameter also includes a second bounded range that is constrained by at least two multiple model curves (e.g., the least and most linear multiple model curves, as claimed in dependent claims 2, 10, 16, 37 and 41 and independent claim 42).

Therefore, independent claims 1, 9, 14, 19, 24, 36, 40 and 42 are patentable over Hershenson in combination with Krivokapic. Furthermore, dependent claims 2-3, 5-8, 10-11, 13, 15-18, 20-22, 25-35, 37-39 and 41 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

III. Formal Matters and Conclusion

With respect to the objections/rejections to the claims, the claims have been amended, above, to overcome these objections/rejections. In view of the foregoing, Applicants submit that claims 1-3, 5-11 and 13-42, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. Therefore, the Examiner is respectfully requested to reconsider and withdraw the objections/rejections to the claims and to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 3/27/07

Pamela M. Riley, Esq.
Registration No. 40,146

Gibb & Rahman, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-0227
Fax: (301) 261-8825
Customer Number: 29154